Single pairing spike-timing dependent plasticity in BiFeO3 memristors with a time window of 25ms to 125µs

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Abstract
Memristive devices are popular among neuromorphic engineers for their ability to emulate forms of spike-driven synaptic plasticity by applying specific voltage and current waveforms at their two terminals. In this paper, we investigate spike-timing dependent plasticity (STDP) with a single pairing of one presynaptic voltage spike and one postsynaptic voltage spike in a BiFeO$_3$ memristive device. In most memristive materials the learning window is primarily a function of the material characteristics and not of the applied waveform. In contrast, we show that the analog resistive switching of the developed artificial synapses allows to adjust the learning time constant of the STDP function from 25ms to 125µs via the duration of applied voltage spikes. Also, as the induced weight change may degrade, we investigate the remanence of the resistance change for several hours after analog resistive switching, thus emulating the processes expected in biological synapses. As the power consumption is a major constraint in neuromorphic circuits, we show methods to reduce the consumed energy per setting pulse to only 4.5 pJ in the developed artificial synapses.

1. Introduction
Since the discovery of spike-timing dependent plasticity (STDP) in biological synapses [Bi and Poo 1998, Di Lorenzo and Victor 2013, Snider 2008], scientists have been captivated by the idea of
changing the synaptic weight, i.e. the strength between the pre- and postneuron, in bioinspired electronic systems in a fashion similar to biology [Indiveri 2006]. However, the circuit-oriented approach is complicated because the ‘synaptic weight’ variable has to be stored typically either as charge in a capacitor [Koickal et al. 2006] or even digitally in neuromorphic IC [Schemmel et al. 2012, Mayr et al. 2013]. This adds circuit complexity and increases energy consumption [Anantharayanan et al. 2009, Adee 2009, Indiveri 2006]. Therefore, nonvolatile analog resistive switches, namely resistive random-access memory (RRAM) or memristors [Chua 1971, Du et al. 2013], responding to well-defined input signals by suitably changing their internal state (‘weight’) are currently developed. For example, the emulation of STDP with 60-80 pairings of pre- and postsynaptic spikes has been shown for artificial synapses based on memristive TiOx [Seo et al. 2011, Thomas and Kaltschmidt 2014], WOx [Chang et al. 2011], HfOx [Yu et al. 2011], GST [Kuzum et al. 2012], and on the memristive BiFeO3 [Cederström et al. 2013, Mayr et al. 2012].

Fig. 1 (A) Schematic illustration of the memristor-based synaptic electronics. The artificial synapses are placed between Integrate & Fire neurons (I&F neuron). With a well-defined time delay $\Delta t$ between the pre- and postspikes the internal state (‘weight’) of the memristor is suitably changed. (B) Hysteresis current-voltage (IV) characteristics of a Au/BiFeO3/Pt memristor in LRS and HRS with a top electrode area of 4.5E4 $\mu$m$^2$ under source voltages with maximum sweeping pulse amplitude of 8.5 V and a pulse width of 100 ms. The current in high resistance state $I_{HRS}$ and in low resistance state $I_{LRS}$ is read out at +2.0 V, after having switched the memristor into HRS and LRS, respectively. The long term potentiation current $I_{LTP}$ and the long term depression current $I_{LTD}$ lie below the reading current in LRS ($I_{LRS}$) and HRS ($I_{HRS}$). Inset shows the structure of a BFO memristor. (C) Schematic demonstration of the distribution of fixed Ti$^{4+}$, fixed Fe$^{3+}$ and mobile V$^{0+}$. Adapted from Reference [You et al., 2014].
Fig. 1A shows a memristor between the electrical Integrate & Fire (I&F) neurons. The synaptic weight of the memristor can be controlled by the time delay $\Delta t$ between pre- and postsynaptic spikes from the 1st layer I&F neuron (Fig. 1A) [Zamarreño-Ramos et al. 2011]. The 2nd layer I&F neuron sums up the signals from all incoming neurons and generates voltage spikes transmitted to other neurons (not shown) through memristor-based artificial synapses. The memristive BiFeO$_3$ (BFO) can serve as an analog resistive switch [Shuai et al. 2011] with multiple distinguishable low resistance states (LRSs) [Shuai et al. 2013, Jin et al. 2014] and with a single detectable high resistance state (HRS). Due to the thermal diffusion of Ti atoms and their substitutional incorporation into the lower part of the BiFeO$_3$ (BFO) layer during BFO thin film growth on a Pt/Ti bottom electrode, the barrier at the Pt/Ti bottom electrode is flexible.

Earlier we have shown that STDP and triplet plasticity with learning windows on the millisecond time scale can be faithfully emulated on BFO-based artificial synapses by applying 60-80 pairings of pre- and postsynaptic spikes [Mayr et al. 2012, Cederström et al. 2013]. In this work we investigate a significantly wider range of timescale configurability, ranging from 25ms to 125μs. To the best of our knowledge, this kind of timescale configurability has not been shown in memristive synapses before. We also examine the evolution of the induced memristive weight change over time and provide several power consumption figures. By increasing the programming voltage (HRS/LRS writing pulse amplitude), it is possible to decrease the switching pulse width as well as the power consumption during a single STDP writing process on BFO-based artificial synapses. Furthermore, the increased programming voltage also shortens the total pairing spike time, and enables to move from the standard biology-like 60-80 spike pairing STDP experiment to a single pairing STDP experiment that results in the same weight/memristance change.

Our work is structured as follows: In Sect. 2, we describe the nonvolatile resistive switching of BFO-based artificial synapses and introduce the single pairing STDP pulse sequence. In Sect. 3, we present the measured learning window, memory consolidation, and energy consumption of the single pairing STDP in BFO-based artificial synapses and discuss configurability, energy consumption, and retention of weight change in Sect. 4. The paper is summarized and an outlook is given in Sect. 5.

2. Materials and methods

2.1. Nonvolatile, analog resistive switching in BiFeO$_3$

Polycrystalline, 600 nm thick BiFeO$_3$ (BFO) thin films with a flexible bottom barrier have been grown by pulsed laser deposition on Pt/Ti/SiO$_2$/Si substrates. Circular Au top contacts have been magnetron sputtered on the BFO thin films using a shadow mask [Shuai et al. 2011, Shuai et al. 2013, Jin et al. 2014]. The Pt/Ti bottom electrode and the Au top contacts posses a flexible and a fixed barrier height, respectively. As illustrated in Fig. 1B, by applying the sweeping source voltage from 0 V -> -8.5 V -> +8.5 V -> 0 V between the Au top electrode and the bottom electrode, the current-voltage characteristics, which were recorded using a Keithley source meter 2400, reveal reproducible nonvolatile hysteretic bipolar resistive switching in BFO memristors with mobile donors (oxygen vacancies) and fixed donors (Ti donors). As illustrated in Fig. 1C which has been adapted from Ref. [You et al. 2014], the physical mechanism underlying resistive switching in BFO memristors is related with the nonvolatile change of flexible barriers in Ti-containing BFO memristors. Due to voltage application of a LRS writing pulse, fixed Ti donors close to the bottom electrode can effectively trap mobile oxygen vacancies in BFO. The bottom electrode becomes non-rectifying and the BFO memristor is in LRS. On the other hand, when applying the HRS switching pulse, the mobile donors in BFO memristors are redistributed between the top and the bottom electrode. The bottom electrode becomes rectifying and the BFO memristor is in HRS. Note that for both writing pulses the Au top electrode remains rectifying.
A single writing pulse with an amplitude $V_w = +8.0$ V and $-8.0$ V can be used to switch the BFO memristor into LRS and HRS, respectively. The maximum possible amplitude increases with the thickness of the BFO memristor and decreases with the length of the writing pulse. For a BFO layer thickness of 600 nm and a writing pulse length of 100 ms, the barrier height of the bottom electrode typically starts to change at a writing pulse of amplitude $V_w = +3.0$ V. Applying a dc voltage below $+2.0$ V to the BFO memristor does not change the barrier height of the bottom electrode, and the state of the BFO memristor does not change. Therefore, the $+2.0$ V dc voltage is defined as the reading bias for the 600 nm thick BFO memristor. The ratio between the resistance $R_{HRS}$ in HRS and the resistance $R_{LRS}$ in LRS amounts to $R_{HRS}/R_{LRS} = 2770$ (Fig. 1B). For changing the synaptic weight the absolute value of the amplitude $V_p$ of the presynaptic and postsynaptic spike has to be larger than the reading bias amplitude $+2.0$ V [Borghetti et al. 2009, Smerieri et al. 2008, Lai et al. 2009]. In our previous work, we used a 500 nm thick BFO layer and an amplitude of $2.3$ V and $2.0$ V for STDP with 60-80 pairings of pre- and postsynaptic spikes. In this work, we use a 600 nm thick BFO layer and an amplitude $V_p$ of $3.0$ V for STDP with single pairing of pre- and postsynaptic spikes. For the potentiating (depressing) spike sequence, the long term potentiation current $I_{LTP}$ (long term depression current $I_{LTD}$) decreases exponentially with decreased pulse amplitude in positive (negative) voltage range: $I_{LRS} > I_{LTP}$ ($I_{HRS} < I_{LTD}$).

Fig. 2 (A) Retention test with a reading bias of $V_r = +2.0$ V after setting the BFO memristor to LRS (red symbols) and to HRS (blue symbols). The reading current has been recorded every 30 s. (B) Retention of multilevel resistive switching in a BFO memristor, which has been initially set to HRS by a writing voltage of $V_w = -8.0$ V. The reading current has been measured at a small reading bias of $V_r = +2.0$ V directly after switching BFO into one of the multiple LRSs with a positive writing bias of $V_w$ ranging from $+2.0$ V to $+8.0$ V (top edge of the rectangles, $t_w = 2$ s) and 30 minutes later (bottom edge of the rectangles, $t_w = 30$ min). Note that the reading current starts to increase for a writing voltage of ca. $+3.0$ V, i.e. the state of the BFO starts to change. All states in Fig. 2B are read with a pulsed reading bias amplitude of $V_r = +2.0$ V and length 100 ms. Because the reading current changes from $I_r = 1.1E-2$ μA in HRS with $R = 1.8E8$ Ω to $I_r = 2$ μA in LRS with $R = 1E6$ Ω, the power ($P = R \cdot I^2$) will change from $2.2E-8$ W in HRS to $4.0E-6$ W in LRS. The resolution of a pulsed power meter amounts to 0.01 dB. So theoretically more than 2000 power levels would be achievable, and we expect that at least 32/64 levels are possible in a power efficient manner.

The nonvolatile resistive switching of BFO was examined by a retention test (Fig. 2A). A single writing pulse of $V_w = +8.0$ V and $-8.0$ V and a pulse width of $t_p = 100$ ms was used to switch the BFO memristor into LRS and HRS, respectively. The reading currents have been read out with a reading bias of $V_r = +2.0$ V and are defined as the current of HRS ($I_{HRS}$) and LRS ($I_{LRS}$). As shown in
Fig. 2A the BFO memristor exhibits degradation of the LRS within the testing time of 2 hours. No significant change has been observed for HRS during the retention time of 5 hours. This non-ideal retention motivated us to investigate memory consolidation [Clopath et al. 2008] in BFO with the shortened pulse sequence of single pairing STDP.

A BFO memristor with multilevel resistive switching can be considered as an analog resistive switch and used as an artificial synapse. The retention of multilevel resistive switching is illustrated in Fig. 2B. Positive writing pulses ranging from 2.0 V to 8.0 V are applied to the BFO-based artificial synapse. As expected from the current-voltage characteristics (Fig. 1B), the reading current at 2.0 V increases with increasing amplitude of the writing bias. After applying the positive writing pulses $V_w$ (as switched, $t_w = 2$ s), the reading current was largest and slightly decreased (30 mins, $t_w = 30$ min) with increasing waiting time $t_w$ (Fig. 2B). However, due to the degradation (Fig. 2B) different LRSs will become indistinguishable. E.g. the reading current for a writing bias of $V_w = 5.5$ V and a waiting time of $t_w = 2$ s is the same as the reading current for $V_w = 6.0$ V and $t_w = 30$ min. We have already shown that the retention of BFO memristors can be significantly improved by an additional BFO surface modification using low energy Ar$^+$ ion irradiation before depositing the Au top electrode [Shuai et al. 2011]. Optimized parameters for the Ar$^+$ irradiation process are discussed in Ref. [Ou et al., 2013]. The Ar$^+$ irradiation helps to homogenize the average crystallite size in the polycrystalline BFO memristors.

### 2.2 Pulse sequence for single pairing spike-timing dependent plasticity

In our previous work, we have used a bias amplitude of $V_p = 2.3$ V for STDP with 60-80 pairings of pre- and postsynaptic spikes [Mayr et al. 2012, Cederström et al. 2013]. Especially, Mayr et al. illustrates how the pre- and postsynaptic waveforms of a specific biology-derived synaptic plasticity rule [Mayr and Partzsch 2010] can be adjusted to operate the BFO memristors. The resulting waveforms are comparable to the waveforms proposed by Zamarreno-Ramos et al. [Zamarreno-Ramos et al. 2011]. In order to shorten the total pairing spike time, in this work we slightly increased the bias amplitude to $V_p = 3.0$ V and applied a single pre- and postsynaptic spike. In comparison to what is discussed in [Mayr et al. 2012], the single spike pairing instead of multiple (60-80) pairings allows us to shorten the total spike time and to adjust the learning time constant of the STDP function from 25 ms to 125 μs. The detailed signal scheme of Memristor initialization, single pairing STDP, and memory consolidation for long term potentiation (LTP) and long term depression (LTD) are shown in Fig. 3. In order to facilitate reproducing this signal scheme, the parameters used in every step in the pulse sequence are listed in Tab. 1. As illustrated in Fig. 6A the signal scheme for resistive switching from HRS into a single LRS (Fig. 6B) can be simplified and reduced to Memristor initialization for LTP and to Memory consolidation for LTD (Fig. 6A). The step labeled Memristor initialization refers to the application of a writing pulse to set the BFO memristor in HRS and LRS. In the HRS the BFO memristor has both rectifying top and bottom electrodes whereas in the LRS the BFO memristor has a rectifying top electrode and a non-rectifying bottom electrode [You et al. 2014]. For the pulse order leading to potentiation (Fig. 3A), a single negative pulse, i.e. the HRS writing pulse, is applied to switch the memristive device into HRS. After the waiting time $t_w$ a single pre- and a single postspike is applied to the top electrode of device. The pre- and postspikes superimpose at the BFO memristor as potentiating spike, and the spike timing difference $\Delta t$ determines the waveform of the potentiating spike ($\Delta t \geq t_p > 0$ for the potentiating inputs). Each pre- and postspike consists of one rectangular pulse with pulse amplitude $V_p$ and one exponentially decaying pulse $V_{exp}$

$$V_{exp} = |V_p| \cdot exp \left( \frac{-t}{\tau} \right),$$  \hspace{1cm} (1)
with the decay time $\tau = \tau_{\text{pre}} = \tau_{\text{post}}$, where $\tau_{\text{pre}}$ and $\tau_{\text{post}}$ are the exponential decay times of pre- and postspikes, respectively. In order to reduce the influence of the exponential decay on the single pairing STDP function, we choose $\tau = 2.5 \cdot t_p$. For the potentiating (depressing) spike order, the spike timing difference $\Delta t$ between the pre- and postspike is positive (negative) and lies in the range: $t_p \leq |\Delta t| \leq 10 \cdot t_p$. In both pre- and postspikes, the rectangular pulse is short compared to the decay time of the exponential waveform, and the amplitude of the overlapped spike pulses depends on the spike time difference $\Delta t$ between both waveforms. After the measurement waiting time $t_w$ the synaptic weight of BFO-based artificial synapses has been checked by applying a reading bias of $V_r = +2.0$ V with a pulse width of $t_r = 100$ ms. The reading current is defined as the potentiation current $I_{\text{LTP}}$ and depression current $I_{\text{LTD}}$ after sourcing potentiating spike and depressing spike, respectively.

Fig. 3 Signal scheme of Memristor initialization, Single pairing STDP, and Memory consolidation. (A) A pre-post spike order is used for long term potentiation (LTP). (B) A post-pre spike order is used for long term depression (LTD). The potentiation current $I_{\text{LTP}}$ (depression current $I_{\text{LTD}}$) and the initial HRS current $I_{\text{HRS}}$ (and the initial LRS current $I_{\text{LRS}}$) are used to normalize the long term potentiation current $\Delta I_{\text{LTP}}$ (the long term depression current $\Delta I_{\text{LTD}}$) as defined in Eq. (2) (Eq. (3)). $t_p$ is the pulse width and $t_w$ is the measurement waiting time before applying the reading pulse $V_r$.

Finally, the reading current $I_{\text{HRS}}$ ($I_{\text{LRS}}$) of BFO in HRS (LRS) is measured at a reading bias of $V_r = +2.0$ V after recording $I_{\text{LTP}}$ ($I_{\text{LTD}}$). For biological reasons it is desirable to keep STDP bounded.
Therefore, we have normalized the LTP and LTD current values. After a potentiating spike sequence the synaptic weight scales with the normalized potentiation current $\Delta I_{LTP}$

$$\Delta I_{LTP}(\%) = \frac{I_{LTP} - I_{HRS}}{I_{LTP}} \times 100\%,$$ (2)

and after a depressing spike sequence the synaptic weight scales with the normalized depression current $\Delta I_{LTD}$

$$\Delta I_{LTD}(\%) = \frac{I_{LTD} - I_{LRS}}{I_{LRS}} \times 100\%.$$ (3)

After normalization using Eq. (2) and Eq. (3) LTP lies in the range from 0% to +100% and LTD lies in the range from 0% to -100%, respectively. As we have shown in [Mayr et al 2012], the specific STDP characteristics can be configured through the waveform. Specifically, $\tau_{pre}$ directly translates to the STDP pre-post time window, while $\tau_{post}$ translates to the post-pre time window. The $V_p$ of the pre and post pulses translate to the respective scaling of the STDP amplitudes.

Table 1. Parameters for the potentiating spike sequence ($\Delta t > 0$) and for the depressing spike sequence ($\Delta t < 0$) during Memristor initialization, Memory consolidation, and Single pairing STDP. The amplitude $|V_w|$ and the length $t_p$ of the writing bias pulse determine the Memristor initialization. The waiting time $t_w$ after Memristor initialization, the waiting time $t_w$ after Single pairing STDP and the amplitude $|V_r|$ and the length $t_r$ of the reading bias pulse determine Memory consolidation. The amplitude $-V_p$, the length $t_p$, the amplitude $+V_p$ and exponential decay $\tau$ determine the presynaptic spike and the amplitude $+V_p$, the length $t_p$, the amplitude $-V_p$, and the exponential decay $\tau$ determine the postsynaptic spike. The time delay between the pre- and the postspike is defined by $\Delta t$.

<table>
<thead>
<tr>
<th>Step in pulse sequence</th>
<th>Memristor initialization</th>
<th>Memory consolidation</th>
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<th>Memory consolidation</th>
<th>Memory consolidation</th>
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<tr>
<td>Potentiating spike sequence</td>
<td>$-V_w &amp; t_p$</td>
<td>$t_w$</td>
<td>$-V_p &amp; t_p / +V_p &amp; \tau$</td>
<td>$t_w$</td>
<td>$+V_r &amp; t_r$</td>
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<tr>
<td>Depressing spike sequence</td>
<td>$+V_w &amp; t_p$</td>
<td>$t_w$</td>
<td>$+V_p &amp; t_p / -V_p &amp; \tau$</td>
<td>$t_w$</td>
<td>$+V_r &amp; t_r$</td>
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<td>$\Delta t &gt; 0$</td>
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3. Results

In the following single pairing STDP in BFO-based artificial synapses (Sect. 2.1) is demonstrated by using different pulse widths $t_p$ and measurement waiting times $t_w$. The potentiating and depressing input signals (Sect. 2.2) have been generated with an Agilent pulse function arbitrary generator 81150A. The reading current has been measured with a Keithley 2400 source meter.

3.1. Learning window

According to the input signal scheme (Fig. 3) the BFO memristor is set in the HRS and in the LRS with a writing pulse amplitude of $V_w = -8.0$ V and $V_w = +8.0$ V, respectively. For the single pairing STDP measurements on a BFO-based artificial synapse pre- and postspikes of different pulse widths $t_p = 10$ ms, 1 ms, 500 μs, and 50 μs, and with a pulse amplitude of $|± V_p| = 3.0$ V, and a waiting time $t_w 10$ s have been chosen (Fig. 4). The exponential decay time constant ($\tau = 2.5 \cdot t_p$) amounts to $\tau = 25$ ms (Fig. 4A), 2.5 ms (Fig. 4B), 1.25 ms (Fig. 4C), and 125 μs (Fig. 4D). After recording $I_{LTP}$ ($I_{LTD}$) the reading current $I_{HRS}$ ($I_{LRS}$) of BFO in HRS (LRS) has been measured at a reading bias of $V_r = +2.0$ V and the normalized potentiation current $\Delta I_{LTP}$ (Eq. 2) and the normalized depression current $\Delta I_{LTD}$ (Eq. 3) are calculated. The synaptic weight of the BFO memristor scales with the normalized potentiation current $\Delta I_{LTP}$ and the normalized depression current $\Delta I_{LTD}$. If the prespike precedes the postspike ($\Delta t > 0$) biological synapses [Bi and Poo 1998] undergo long term potentiation LTP, i.e. the connection between two neurons becomes stronger. On the other hand, if the postspike precedes the

![Fig. 4 Long term depression current $\Delta I_{LTD}$ (negative range of y-axis) and long term potentiation current $\Delta I_{LTP}$ (positive range of y-axis) of a ca. 600 nm thick BFO memristor with a contact area of 4.5E4 μm² for single pairing STDP with pulse width (A) $t_p = 10$ ms, (B) $t_p = 1$ ms, (C) $t_p = 500$ μs and (D) $t_p = 50$ μs, measurement waiting time $t_w = 10000$ ms, pulse amplitude $V_p = 3.0$ V, reading pulse amplitude $V_r = +2.0$ V and reading pulse width $t_e = 100$ ms. $\Delta I_{LTD}$ and $\Delta I_{LTP}$ have been normalized using Eq. (2) and Eq. (3), respectively. The memristor was preset in HRS and LRS (Memristor initialization in Tab. 1) with a writing pulse amplitude of $V_w = -8.0$ V and $V_w = +8.0$ V, respectively.]

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In the following single pairing STDP in BFO-based artificial synapses (Sect. 2.1) is demonstrated by using different pulse widths $t_p$ and measurement waiting times $t_w$. The potentiating and depressing input signals (Sect. 2.2) have been generated with an Agilent pulse function arbitrary generator 81150A. The reading current has been measured with a Keithley 2400 source meter.
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prespike (Δt<0), biological synapses undergo long term depression LTD, i.e. the connection between
two neurons becomes weaker. We have measured the LTD current $I_{LTD}$ and the LTP current $I_{LTP}$ in a
BFO-based artificial synapse and can show that the BFO memristor emulates the STDP function of
biological synapses. The normalized current $\Delta I$ decreases with increasing delay time $|\Delta t|$. The
normalized current curve for positive and negative $\Delta t$ is the LTP and LTD curve (Fig. 4),
respectively. As an example, in the following we discuss the LTP curve in Fig. 4 for $\Delta t = t_p > 0$.
Initially the BFO-based artificial synapse is set into HRS. The maximum amplitude of the
potentiating spike amounts to $2V_p = +6.0 \text{ V}$. For this potentiating spike the BFO-based artificial
synapse is fully switched to LRS. The normalized potentiation current $\Delta I_{LTP}$ at $\Delta t = t_p$ amounts to ca. 100 %. In the time delay range $0 < t_p < \Delta t \leq 10 \cdot t_p$, the maximum amplitude of potentiating spikes is reduced from 6.0 V to 3.2 V. Therefore, the exponential-like decay of the normalized current dominates STDP with increasing $\Delta t$ and the synapse cannot be fully switched to LRS by applying these potentiating spikes. For both positive and negative time delays $|\Delta t| = 10 \cdot t_p$, $\Delta I$ decreases with decreasing pulse width $t_p$. At $t_p = 500 \mu \text{s}$ and 50 $\mu \text{s}$, $\Delta I_{LTP}$ amounts to 0% at $|\Delta t| = 10 \cdot t_p$. It is also noticed that $\Delta I_{LTP}$ decreases more strongly than $\Delta I_{LTD}$ in the larger time delay range. That is because the threshold voltage for LRS is higher than the threshold voltage for HRS. For example in Ref. [Mayr et al. 2012] a voltage of 2.3 V and of 2.0 V has been used as the threshold voltage to switch a BFO-based artificial synapse to LRS and HRS, respectively. The shaded regions in Fig. 4 show the ranges of the delay time $\Delta t$ where the normalized current is larger than 50% for four different pulse widths $t_p$. This range is also called learning window and decreases from 25 ms to 125 $\mu \text{s}$ with decreasing pulse width $t_p$ from 10 ms to 50 $\mu \text{s}$.

As can be seen from Fig. 4, the STDP time windows can be finely controlled. Specifically, making $\Delta t$ longer results in a monotonous decrease in both potentiation and depression with increasing $\Delta t$, i.e. the memristance change directly and fine grainedly follows the applied waveform resulting from the overlay of pre- and postpulse. This is in contrast to most other reported memristive synapses, where the time difference between pre- and postpulse only translates to a stochastic, average change of memristance [Jo et al. 2010, Alibart et al. 2012].

Fig. 5 (A) STDP of a BFO-based artificial synapses with different waiting times $t_w = 2 \text{ s}$ (circles), 1 min (quadrangles), and 5 min (triangles) for $t_p \leq \Delta t \leq 10 \cdot t_p$. Pulse amplitude $V_p = 3.0 \text{ V}$, pulse width $t_p = 10 \text{ ms}$, and exponential decay time $\tau = 25 \text{ ms}$. (B) Memristance weight consolidation for a fixed $\Delta t = t_p = 10 \text{ ms}$ and for a waiting time of $t_w = 2 \text{ s}$ (circles), 60 s (quadrangles) and 300 s (triangles) from Fig. 5 (A) and $t_w = 0.5 \text{ h}, 1 \text{ h}, 2 \text{ h}, 3 \text{ h}, 4 \text{ h}, 5 \text{ h}$ (squares). The pulse amplitude $V_p$ amounts to 3.0 V. The exponential decay amounts to $\tau = 25 \text{ ms}$. The writing voltage for Memristor initialization amounts to $|\pm V_W| = 6.0 \text{ V}$. 

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3.2. Memory consolidation

Memory consolidation has been investigated in models of biology in order to improve the understanding of the translation of an initially induced weight change to long term weight stabilization [Clopath et al. 2008, Anokhin 2005]. This motivated us to investigate the memristance weight, i.e. memory consolidation, in BFO-based artificial synapses in more details by performing single pairing STDP measurements with different waiting times \( t_w \) (2 s \( \leq t_w \leq 5 \) h). In biological systems, the waiting time corresponds to the time which elapses before something learned is retrieved. On the other hand, for the memory consolidation measurements, we have again used the ca. 600 nm thick BFO-based artificial synapses and applied a writing voltage of \( V_w = +6.0 \) V. In Fig. 5A the corresponding STDP data are plotted for \( t_w = 2 \) s, 60 s, and 300 s. We have chosen single pre- and postsynaptic spikes with the same absolute value of the pulse amplitude \( V_p = 3.0 \) V, pulse width \( t_p = 10 \) ms and exponential decay time \( \tau = 25 \) ms. As shown in Fig. 5A, the LTP and LTD curves shift towards low normalized current values with increasing waiting time in both positive and negative spike timing ranges. Therefore, the dependence of LTP and LTD on the writing pulse amplitude can be used to trace differences in the LTP and LTD curves of single pairing STDP. For BFO-based artificial synapses with a smaller writing voltage \( V_w \), the optimized STDP curve with more significant exponential-like function (as shown in Fig. 4) is reproducible by choosing a smaller pulse amplitude \( V_p \), e.g. \( V_p = 2.5 \) V.

Fig. 6 (A) Signal scheme for resistive switching a BFO memristor in HRS into LRS. The memristor is initialized into the HRS by applying a writing voltage \( V_w = -6.0 \) V with a pulse width \( t_p = 100 \) ms, and is then switched back to different LRSs with different pulse amplitudes \( V'_w \) and pulse widths \( t'_p \). (B) Reading current of the BFO memristor with a contact area of 4.5E4 \( \mu m^2 \) in LRS in dependence on the writing voltage \( V'_w \) in the range from 6.0 to 23.0 V and with different constant pulse widths of \( t'_p = 50 \) ms, 1 ms, 50 \( \mu s \), 1 \( \mu s \), 500 ns, and 50 ns. The reading voltage amounts to +2.0 V. For a given pulse width at least one writing voltage (red bar) is large enough to set the BFO memristor in the LRS. In that case the reading currents is even larger than the current \( I_{LRS} \) read out after applying a writing voltage of \( V_w = +6.0 \) V with a pulse width of \( t'_p = 100 \) ms (first red bar).
Furthermore, memory consolidation measurements (Fig. 5B) reveal that for a waiting time $t_w$ shorter than one hour there is a visible change of reading current (degradation) both in positive and negative spike timing ranges after applying a single presynaptic and postsynaptic pulse sequence, whereas for a waiting time $t_w$ longer than two hours the current is stabilized. This is in agreement with the results from retention measurements (Fig. 2A).

### 3.3. Energy consumption

Low energy efficiency, large chip size, and complex STDP synapse circuits are major bottlenecks of today’s bio-inspired systems, e.g. neural networks where synapses typically outnumber neurons by more than 500:1. In order to reliably observe STDP functionality the corresponding current changes should lie in the nA current range and above. In addition to the stabilization of multilevel resistive switching, we can also increase the current level in a controlled manner by low-energy Ar$^+$ ion irradiation [Ou et al., 2013]. This will allow for integrating BFO-based artificial synapses with smaller contact area $A$ (Tab. 2), e.g. in neural networks, without adding another device for amplifying current changes. The estimated energy consumption of each synapse in human brain amounts to only $1 \text{ -- } 10 \text{ fJ}$ (Tab. 2). In order to approach the high energy efficiency of biological synapses, we applied single pairing (not 60-80 pairing) STDP pulses to BFO-based artificial synapses. For single pairing STDP most of the energy is consumed during SET operation, e.g. Memristor initialization into LRS (Tab. 1, Fig. 3). For example, in TiN/Ge$_2$Sb$_2$Te$_5$/TiN/W artificial synapses the energy for SET operation is 50 pJ while the energy for RESET operation is 0.675 pJ Ref. [Kuzum et al. 2012].

<table>
<thead>
<tr>
<th>Single Synapse</th>
<th>$E$ (pJ)</th>
<th>$V_w$ (V)</th>
<th>$I_{\text{avg}}$ (µA)</th>
<th>$t_p$ (ns)</th>
<th>$A$ (µm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human brain (total number of synapses $N=10^{15}$, $P_{\text{total}} = 10 \text{ W}$) [Kandel and Schwartz 1985, da Costa 2013]</td>
<td>(1-10) *1E-3</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0.12</td>
</tr>
<tr>
<td>TiN / Ti / AlO$_x$ / TiN / Ti [Wu et al. 2012]</td>
<td>1.5</td>
<td>+1.5</td>
<td>+100</td>
<td>10</td>
<td>0.72</td>
</tr>
<tr>
<td>Au / BFO / Pt / Ti (this paper)</td>
<td>4.7</td>
<td>+23.0</td>
<td>+4.1</td>
<td>50</td>
<td>4.5E+4</td>
</tr>
<tr>
<td>TiN / HfO$_x$ / AlO$_x$ / Pt [Yu et al. 2011]</td>
<td>6.0</td>
<td>-2.5</td>
<td>-240</td>
<td>10</td>
<td>0.0079</td>
</tr>
<tr>
<td>TiN / Ge$_2$Sb$_2$Te$_5$ / TiN / W [Kuzum et al. 2012]</td>
<td>50</td>
<td>-5.5</td>
<td>-900</td>
<td>10</td>
<td>0.018</td>
</tr>
<tr>
<td>CMOS-electrode / Ag + Si / CMOS-electrode [Jo et al.]</td>
<td>430</td>
<td>+3.2</td>
<td>+0.45</td>
<td>3.0E+5</td>
<td>0.031</td>
</tr>
<tr>
<td>Pd / WO$_x$ / W / SiO$_2$ / Si [Chang et al. 2011]</td>
<td>520</td>
<td>+1.3</td>
<td>+0.40</td>
<td>1.0E+6</td>
<td>0.053</td>
</tr>
</tbody>
</table>
The energy consumed during SET operation is
\[ E = V'_w \cdot I_{\text{avg}} \cdot t'_p, \] (4)
with \( I_{\text{avg}} = I_{\text{peak}} / 2 \). The writing voltage amplitude \( V_w \), the setting current \( I_{\text{peak}} \), and writing pulse width \( t_p \) are the crucial parameters for evaluating the energy consumption. Note that for the polycrystalline BFO memristors with different sizes of BFO crystallites, larger BFO crystallites below the top electrode are possibly not switchable. Therefore, the effective area of the top electrode might be smaller than the nominal area of the top electrode. Using BFO-based artificial synapses we can downscale the size of the top electrodes [Jin et al. 2014], increase the pulse amplitude \( V'_w \) and also reduce the pulse width \( t'_p \) (Eq. 4) to further decrease the energy consumption per setting process (Fig. 6).

In order to optimize the energy efficiency of BFO-based artificial synapses, we have applied a large writing pulse amplitude of 23.0 V to compensate the short pulse width of 50 ns. The corresponding energy consumption amounts to 4.7 pJ. The LRS reading current and HRS reading current at 2.0 V amount to 980 nA and 64 nA, respectively. The theoretical maximum normalized current ranges from 93.5% to 0% and from 0% to 93.5% in both curves (Eq. (2), Eq. (3)).

In Table 2 [Chang et al. 2011, Yu et al. 2011, Kandel and Schwartz 1985, Wu et al. 2012, Kuzum et al. 2012, Jo et al. 2010] different memristor-based artificial synapses are listed and compared with respect to their energy consumption per (re)setting process. The TiN / Ti / AlOx / TiN / Ti memristor [Wu et al. 2012] shows the smallest energy consumption of 1.5 pJ per SET pulse. It is expected that to a certain extent the energy consumption can be further reduced by further reducing the electrode area size \( A \). However, one has to consider that BFO is a polycrystalline thin film and that only 1%-0.1% of the crystallites below the top electrode of the polycrystalline BFO are switched in single pairing STDP.

4. Discussion

4.1. Configurability

In this work single pairing STDP in BFO-based artificial synapses has been demonstrated for emulating the functionality and the plasticity of biological synapses. The waveform-defined plasticity of BFO memristors in addition to their multilevel memristive programming capability enables easy control of the STDP time windows, as evidenced by the three orders of magnitude timescale configurability shown in this paper. While there has been a lot of simulation work on this topic, the number of devices where STDP or variations have actually been implemented and measured is still fairly small [Alibart et al. 2012, Jo et al. 2010]. Among those, our highly-configurable, finely grained learning curves are unique, other implementations exhibit statistical variations [Jo et al. 2010], can only assume a few discrete levels [Alibart et al. 2012] or the learning windows are device-inherent, i.e. cannot be adjusted [Ohno et al. 2011]. We expect that for BFO-based artificial synapses at least 32/64 levels are possible in a power efficient manner. In addition, the wide range of timescales possible in BFO-based synapses enables e.g. a timebase-tunable system that could learn a classification offline in an accelerated manner, while still able to interact with real-time sensors before or after this learning.

As mentioned in the introduction, BFO-based artificial synapses can be used for conventional STDP experiments, where only multiple spike pairings exhibit significant weight change, as well as in the mode used in this paper, where a single pairing already induces a significant weight change. By changing the voltage of the pre- and postsynaptic pulses, any point in between these two extremes can also be chosen, again showing the excellent configurability of BFO-based artificial synapses.
However, the versatility of BFO memristors comes at the price that in contrast to *e.g.* phase-change materials, BFO is not easily integrated on top of CMOS [Shuai *et al.* 2013].

### 4.2. Energy consumption

In Tab. 2, we have shown an energy consumption of $E = 4.7$ pJ in a BFO-based artificial synapse with electrode size of $4.52 \times 10^4 \mu$m$^2$. While this is still three orders of magnitude above the energy consumption of biological synapses, it is one of the lowest reported so far for other artificial synapses. Compared to neuromorphic approaches, all memristive approaches are several orders of magnitude better [Azghadi *et al.* 2014]. In terms of absolute area, the BFO memristor is comparable to some neuromorphic implementations [Hasler and Marr 2013, Noack *et al.* 2015], but not competitive with memristor crossbar devices, as we are employing a single device test structure that has a large contact size for reasons of convenience. However, BFO device scaling is well established, thus we can aggressively scale the size of the top electrode to $10 \mu$m$^2$ and the thickness of the BFO to 100 nm [Jin *et al.* 2014]. For BFO with larger electrode area size, the current scales linearly with area size. For smaller electrode area size we would expect that the current scales with the number of BFO crystallites below the electrode. And in the limit case of nanoscale electrodes, the smallest possible current should be the current through single BFO crystallites.

### 4.3. Retention of weight change

We have investigated the retention of memristance weight change across time. As Fig. 5A shows, the basic shape of the STDP curves is preserved across time. Fig. 5B illustrates that even after memory consolidation, we retain a graded weight, *i.e.* a unimodal weight distribution. Our synapse does not collapse in either a potentiated or depressed (bimodal) distribution as predicted in some synaptic models [Fusi *et al.* 2000, Clopath *et al.* 2008]. In memristive literature, there is usually no investigation of these phenomena, the weight change is taken at some unspecified time after induction and then assumed to be non-volatile. Only very few articles have investigated the actual non-volatility/weight retention across time and shown that the assumption of a non-volatile change is not necessarily valid [Chang *et al.* 2011]. Thus, compared to other reports, this article gives a neuromorphic designer a clear guide on how to utilize the memristive synapses for long-term storage. Interestingly, this investigation of memory consolidation is also somewhat missing in the original biological measurements. Usually, data on the weight evolution ca. 30-60 min after induction is provided, but only on single example pairing experiments. These data points show various behaviors, from unchanged weights after initial weight induction [Froemke and Dan 2002] to increases of weight change across time [Bi and Poo 1998], decreases across time [Markram *et al.* 1997] or slow oscillations around the initial potentiated/depressed weight value [Sjöström *et al.* 2001]. However, it is unclear how the overall STDP window consolidates over time. Thus, measuring the evolution of an STDP curve across time after induction at biological synapses similar to our investigation on memristive synapses may actually be a quite interesting scientific question.

### 5. Summary and outlook

In this work we have investigated a wide range of timescale configurability, ranging from 25ms to 125μs. Also, we have investigated power consumption figures and have shown that it is possible to decrease the switching pulse width and to reduce the power consumption during a single STDP writing process on BFO-based artificial synapses to only 4.5 pJ. Furthermore, the increased programming voltage also shortens the total pairing spike time, and enables to move from the
standard biology-like 60-80 spike pairing STDP experiment to a single pairing STDP experiment
with the same weight/memristance change.

One important advantage of single STDP in comparison to 60-80 spike STDP is that both pre- and
postsynaptic waveform are causal, i.e. they start only at the pre- respectively postsynaptic pulse. This
is in contrast to most currently proposed waveforms for memristive learning, where the waveforms
have to start well in advance of the actual pulse [Zamarreño-Ramos et al. 2011], which requires pre-
knowledge of a pulse occurrence. Especially, in an unsupervised learning context with self-driven
neuron spiking, this pre-knowledge is simply not existent.

In a wider neuroscience context, waveform defined plasticity as shown here could be seen as a
general computational principle, i.e. synapses are not likely to measure time differences as in native
forms of STDP rules, they are more likely to react to local static [Ngezahayo et al. 2000] and
dynamic [Dudek and Bear 1992] state variables. In the future some interesting predictions could be
derived from that, e.g. STDP time constants that are linked to synaptic conductance changes or to the
membrane time constant [Pfister et al. 2006, Mayr and Partzsch 2010]. These predictions could be
easily verified experimentally.

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References


Alibart, F., Pleutin, S., Bichler, O., Gamrat, C., Serrano-Gotarredona, T., Linares-Barranco, B., and


Molecular Genetics Neurosciences”. In Complex Brain Functions: Conceptual Advances in
Russian Neuroscience, ed. R. Miller, A. M. Ivanitsky, and P. M. Balaban (Amsterdam, FL:

synaptic plasticity in silicon: Design, implementation, application, and challenges,

Dependence on spike timing, synaptic strength, and postsynaptic cell type. J. Neurosci. 18:
10464-10472.

Borghetti, J., Li, Z., Straznicky, J., Li, X., Ohlberg, D. A. A., Wu, W., Stewart, D. R., and Williams,


Da Costa, N. M. (2013). Diversity of thalamorecipient spine morphology in cat visual cortex and its implication for synaptic plasticity. *Journal of Comparative Neurology 521(9):* 2058-2066.


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Single pairing STDP in BFO-based memristor


Figure 2: 

(A) Reading current in LRS and HRS at \( V_w = +8 \, V \) and \( V_w = -8 \, V \) respectively, with \( V_t = +2 \, V \) at retention time.

(B) Reading current \( I_{LRS} \) as a function of writing voltage \( V_w(V) \), with \( t_w = 2 \, s \) and \( t_w = 30 \, min \) at reading voltage \( V_r = +2 \, V \).
Figure 6. JPEG

(A) HRS writing pulse

- $V_w'$
- $t_p$
- $t_w$
- $t'_p$
- LRS writing pulse
- Reading pulse

(B) @ $V_r = +2 \text{ V}$

- Current (µA)
- Writing voltage $V'_w$ (V)

- $t'_p = 100 \text{ ms, 1 ms, 50 \mu s, 1 \mu s}$
- $t_r = 50 \text{ ns, 500 \mu s, 50 ns}$

LRS

HRS